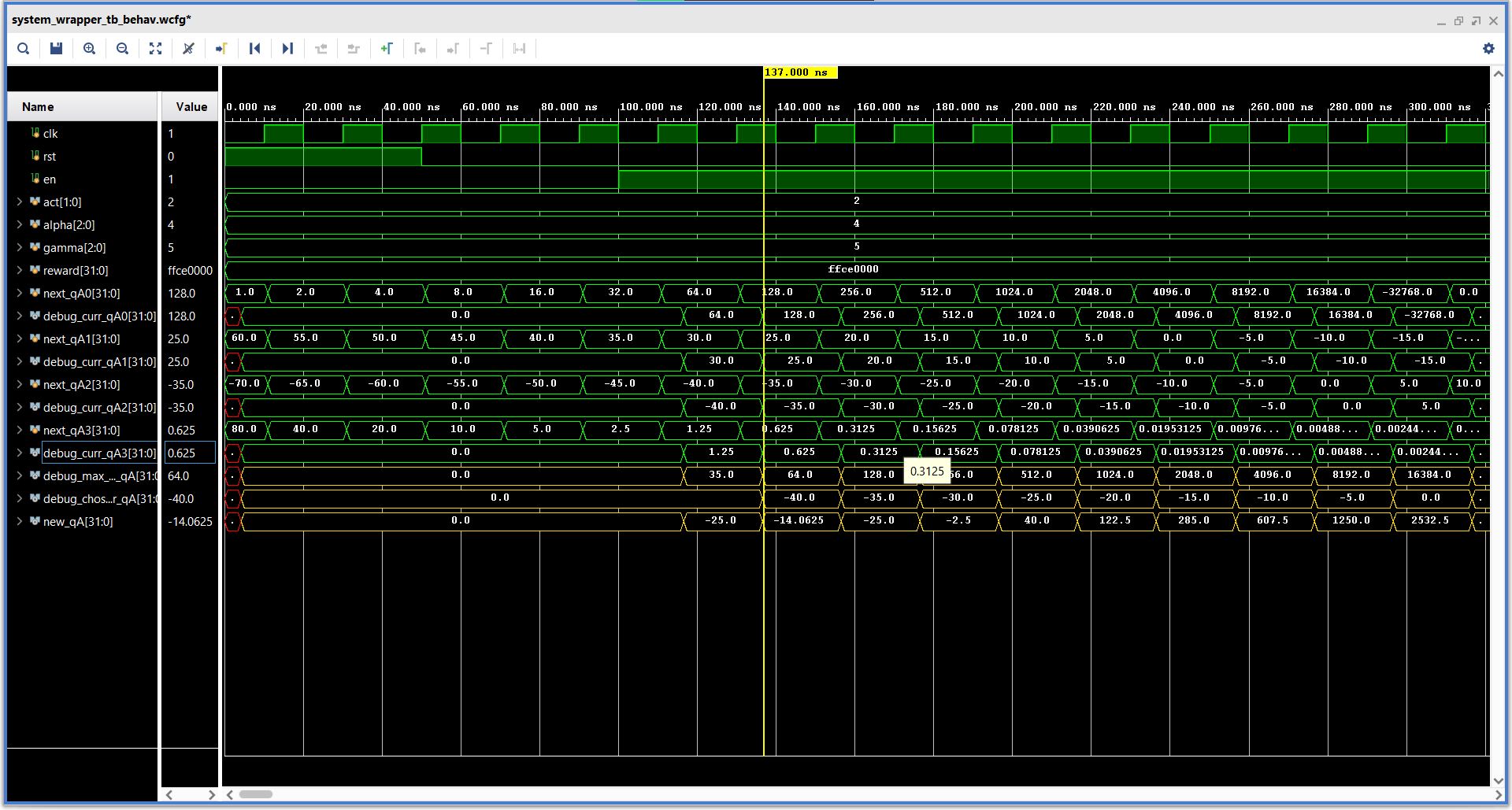
**DATA SIMULASI TIMING**

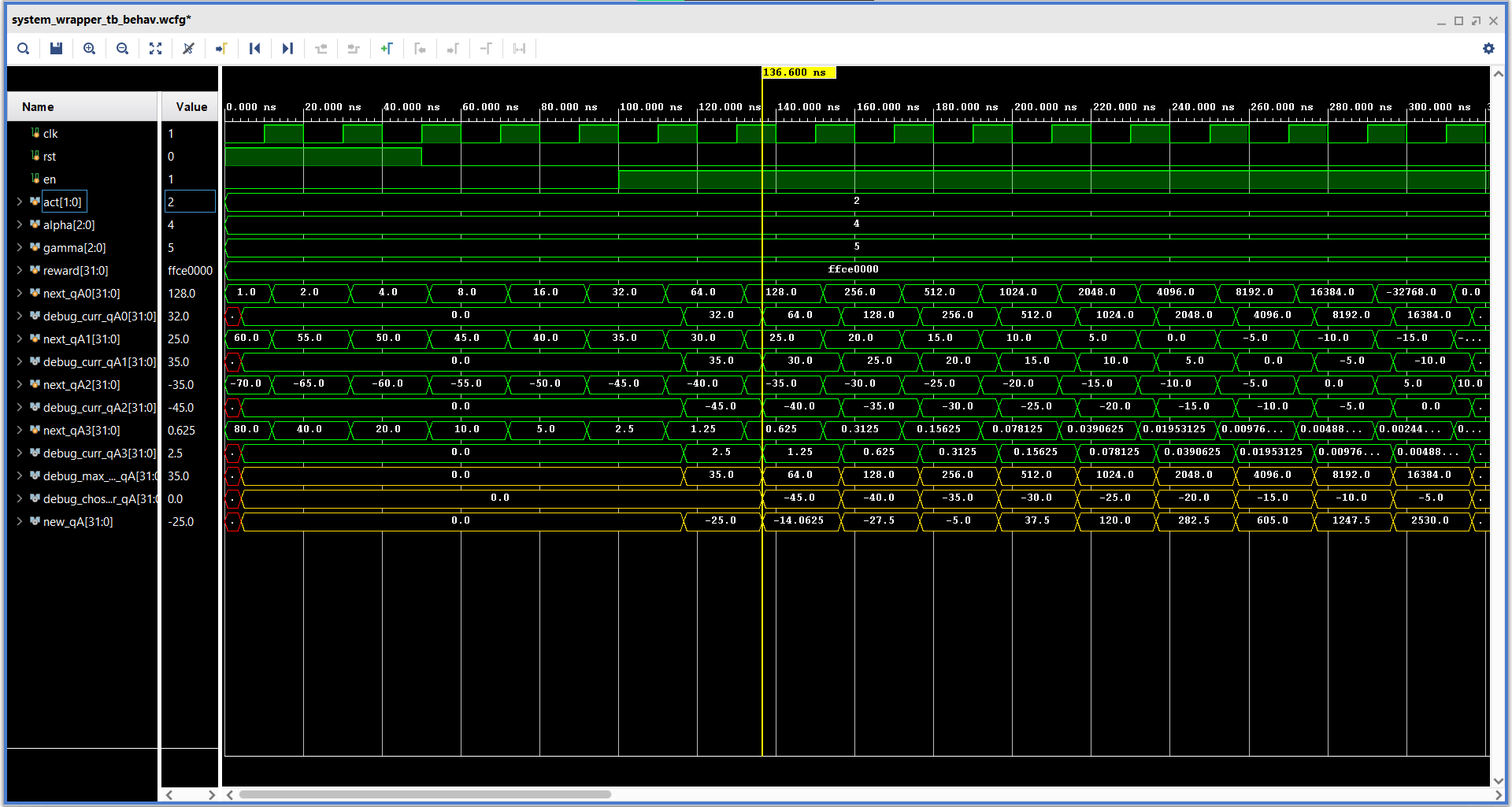
Engineer : Zulfikar

**BLOK Q ACCELERATOR**

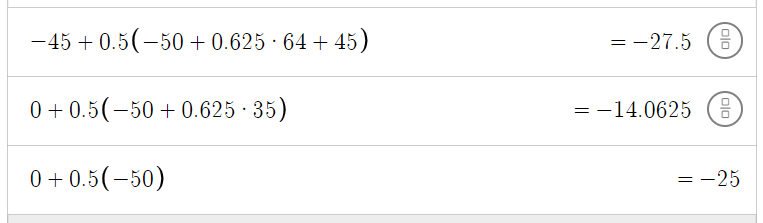
Input terlambat 1 ns



Input terlambat 2 ns



Verifikasi perhitungan :

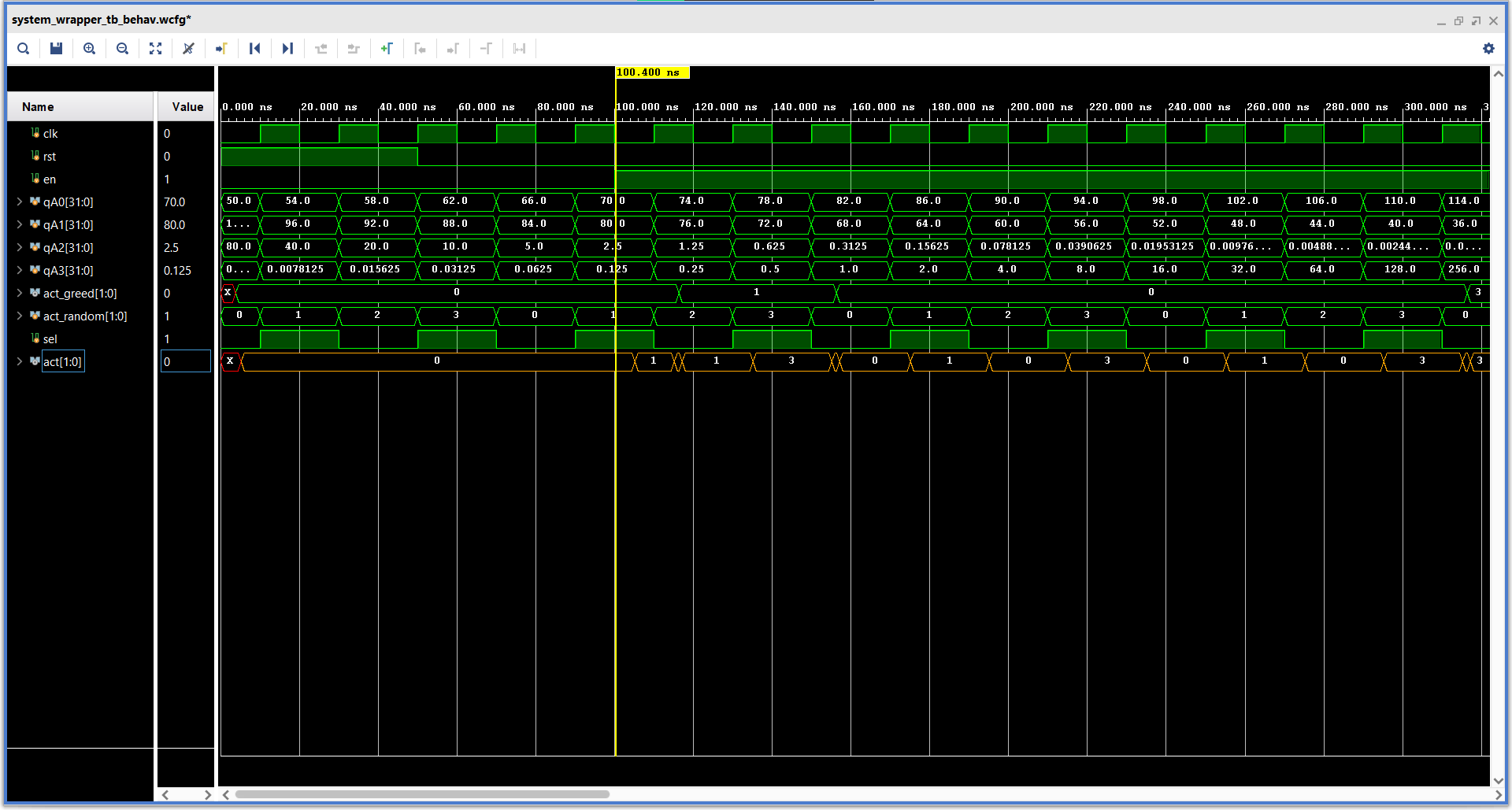


Analisis :

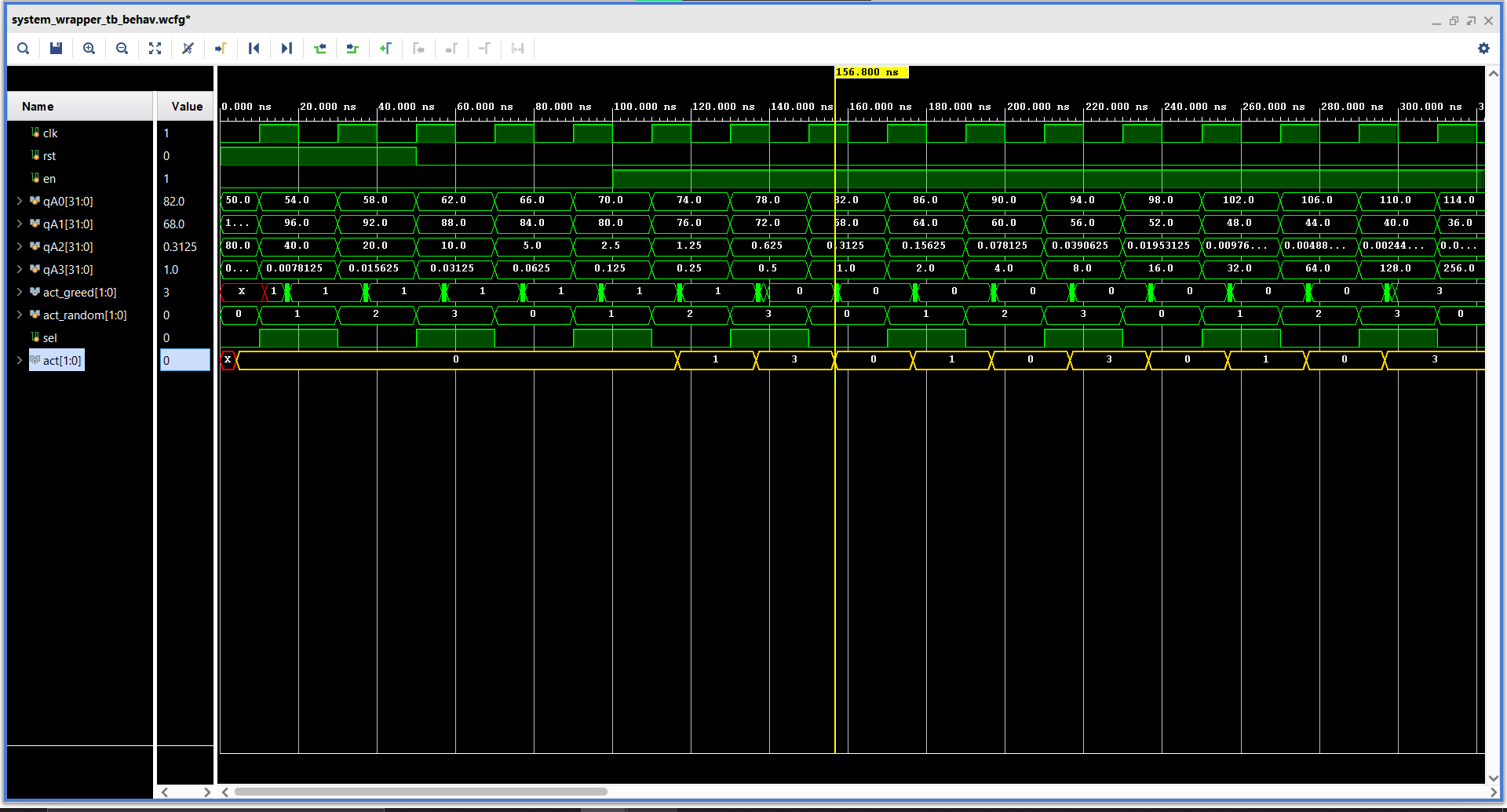
* Timing diagram terpenuhi ketika input terlambat >2 ns
* Langkah perhitungan QA sudah benar

**BLOK POLICY GENERATOR**

Register di output Block Greed Action



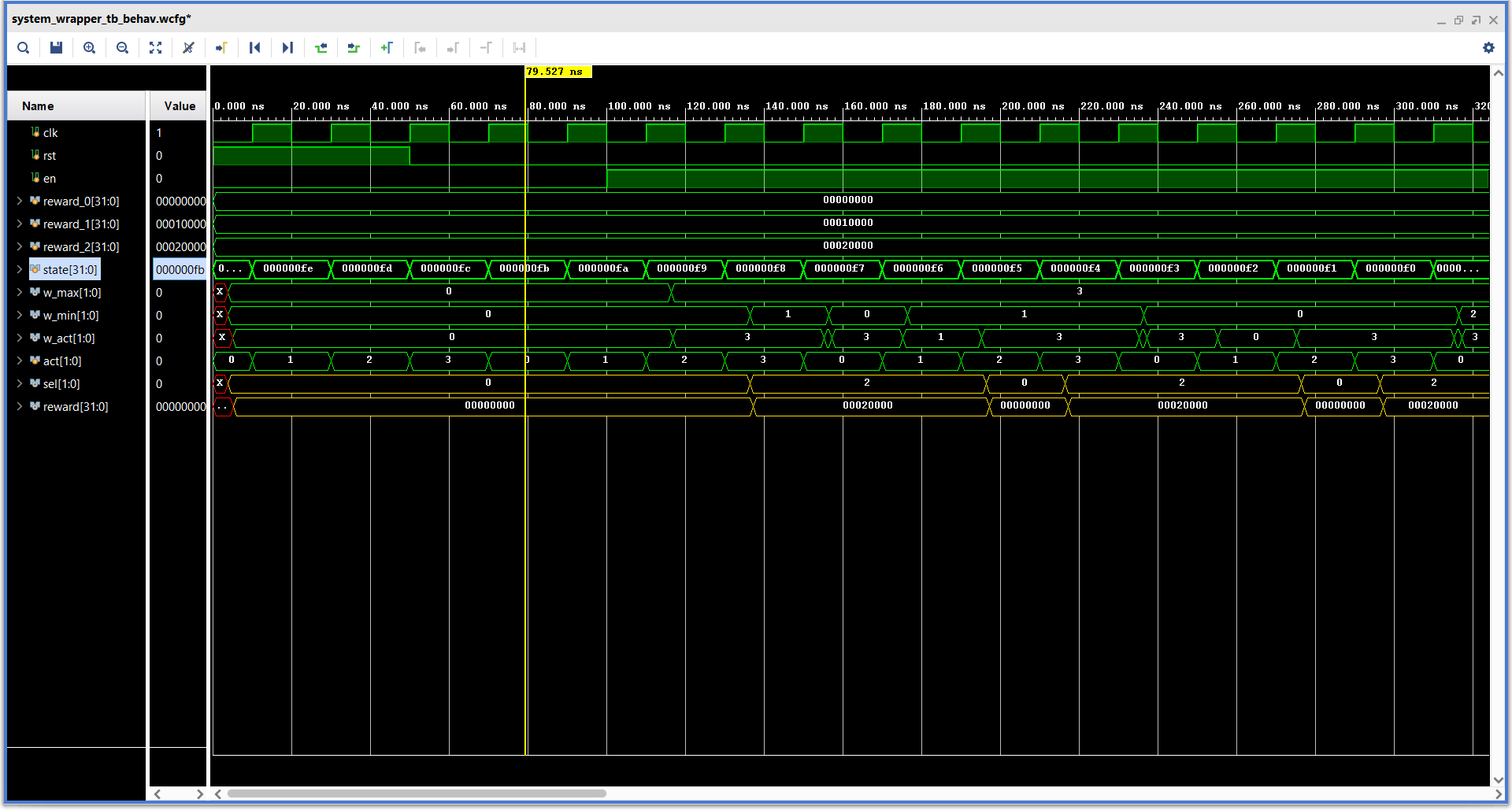
Register di output final

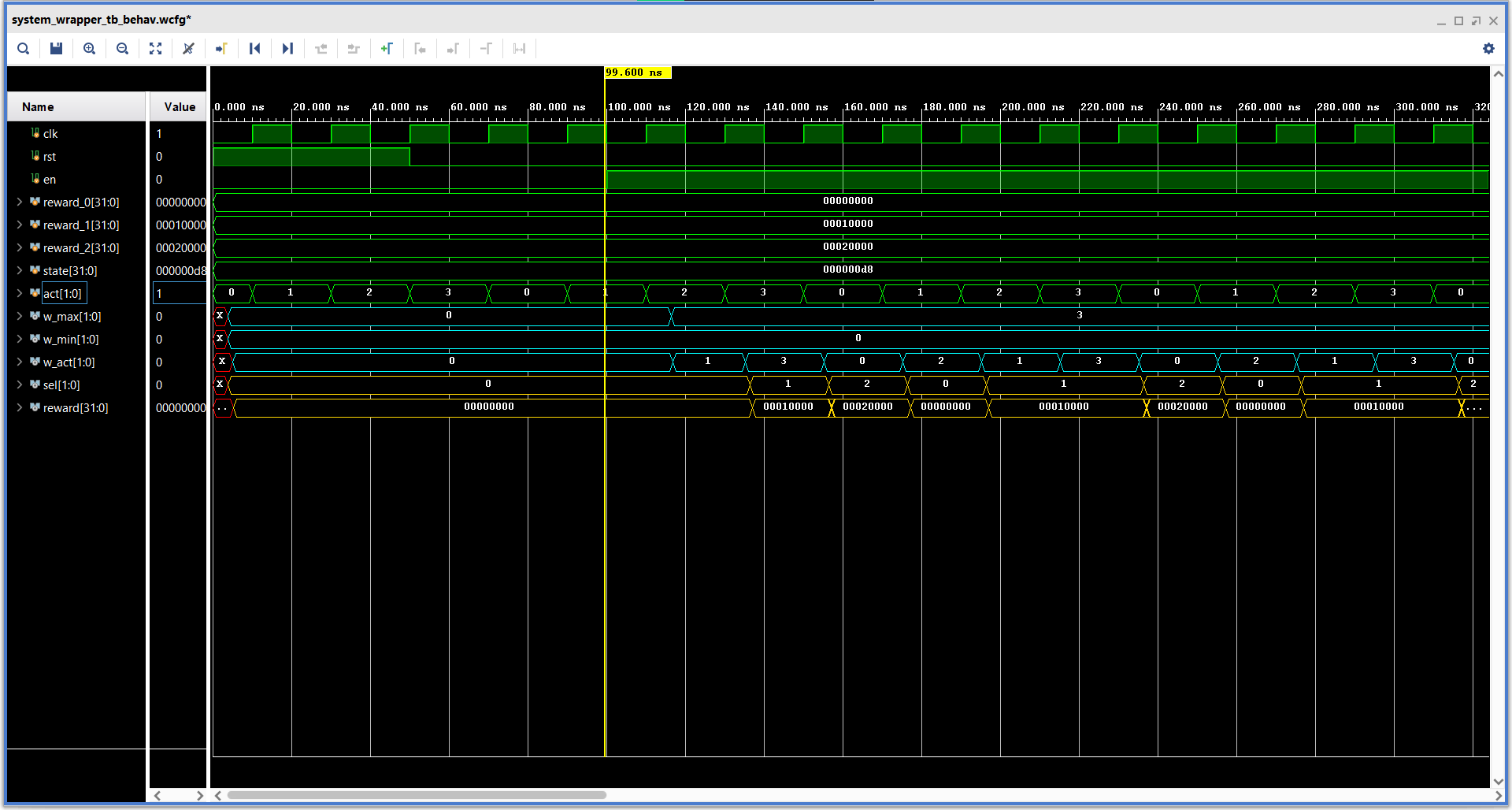


Analisis :

* Ketika register di output blok greed action : action final ada glitch
* Ketika register di output keseluruhan blok : action final tidak ada glitch
* Waktu pemrosesan blok Greed Action 2 ns
* Aman untuk memindah register ke akhir keseluruhan blok

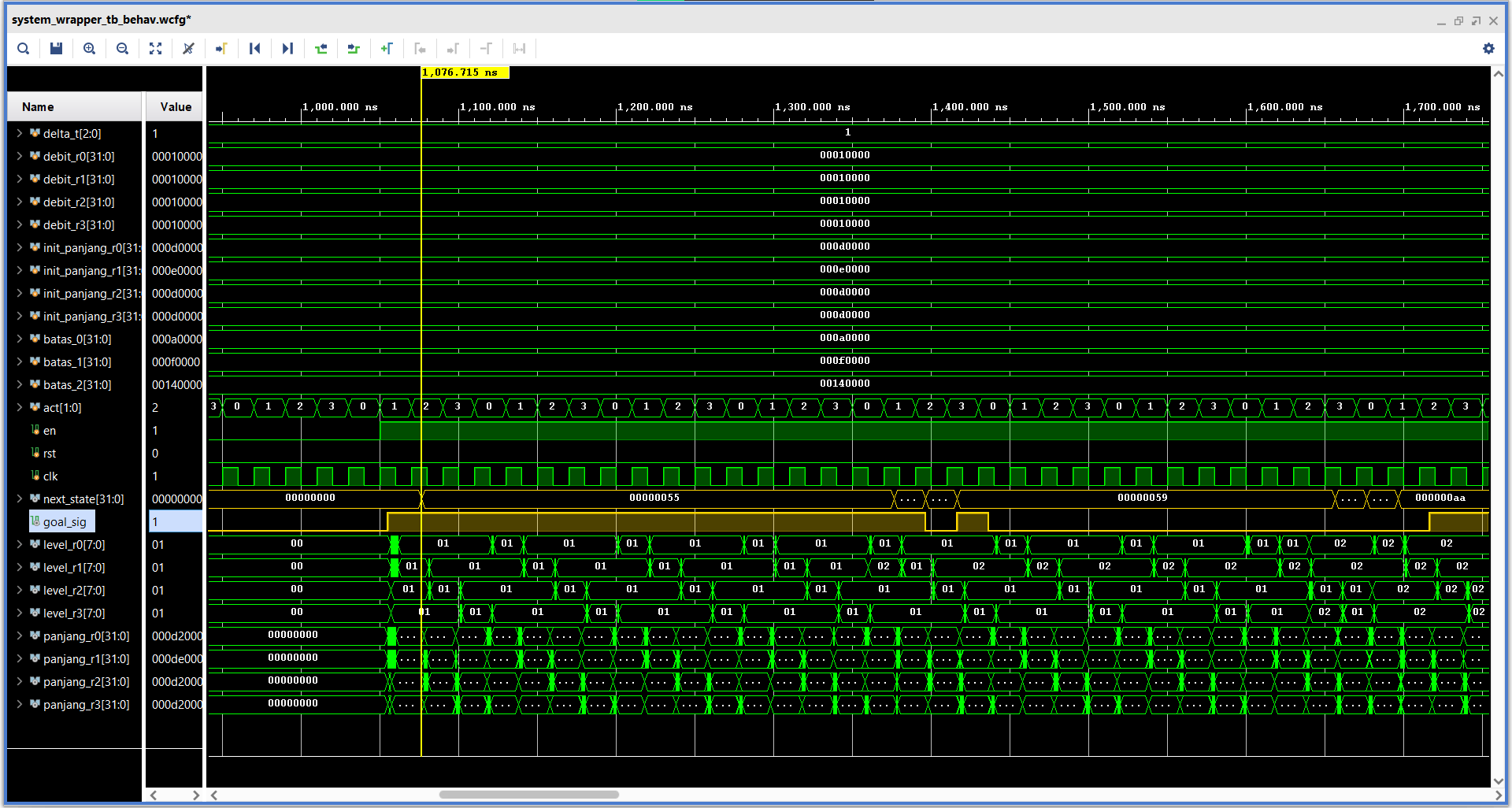
**BLOK REWARD DECIDER**

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****

Sudah aman

**BLOK STATE DECIDER**

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* Respon perubahan state terhadap perubahan level kemacetan = 6 ns
* **Perlu modifikasi timing diagram**karena rangkaian kombinasional terlalu panjang